SOITEC ANNOUNCES ADOPTION OF FULLY DEPLETED TECHNOLOGY FOR ADVANCED MOBILE PLATFORMS

ST-Ericsson selects FD technology for upcoming NovaThor™ high performance, low power application processors

Bernin, France – March 12, 2012 – Soitec (Euronext), a world leader in generating and manufacturing revolutionary semiconductor materials for the electronics and energy industries, announced today that ST-Ericsson, a leader in wireless platforms and semiconductors, has selected planar fully depleted silicon on insulator (FD-SOI) technology for use in future mobile platforms. Soitec's innovative substrates ─ with an extremely thin top layer which predefines critical characteristics of the transistor ─ provide the foundation upon which fully depleted transistors are built.

"Next-generation mobile consumer devices will need to deliver an even better user experience and higher performance without sacrificing battery life," said Louis Tannyeres, chief chip architect, ST-Ericsson. "Together with innovations in overall platform system design, advances in process technology are key to delivering next-level performance and higher power efficiency. The results of our work with STMicroelectronics on FD-SOI have demonstrated that this technology is able to deliver these benefits in a cost-effective manner, while allowing us to differentiate our solutions."

FD-SOI wafers from Soitec enable enhanced performance for NovaThor™ at much lower battery usage – as much as 35 percent lower power consumption at maximum performance. For consumers, this can translate into devices that provide four additional hours of high-speed Web browsing or as much as a day of additional battery life.

"FD provides a low-risk option for semiconductor companies such as ST-Ericsson that are seeking to take advantage of the benefits of a fully depleted transistor architecture while leveraging existing design and manufacturing capabilities," said Paul Boudre, chief operating officer of Soitec. "This announcement represents the industry's first step toward fully depleted planar CMOS technology, years ahead of when alternative processes will be available from foundries. We are positioned to provide the volume of qualified wafer manufacturing required to enable the industry to speed the adoption of planar fully depleted technology into mainstream mobile applications."

"STMicroelectronics and its partners Leti, Soitec and IBM have invested several years of development in FD-SOI technology, and ST has recently demonstrated the strong differentiation of this technology versus conventional bulk CMOS, both for high-performance and low-power features on several IPs at 28nm and below," said Joël Hartmann, STMicroelectronics assistant general manager, Technology R&D. "This combination makes FD-SOI particularly suitable for

wireless and tablet applications where it essentially provides the fully depleted transistor benefits of FinFETs on a planar conventional technology, while allowing advanced back bias techniques, which are not available with FinFETs. We are delighted that it could be adopted by ST-Ericsson for their next generation of products."

As innovative form factors push semiconductor manufacturers to move beyond 28nm process nodes, it is becoming clear that traditional bulk CMOS process technology cannot balance these attributes effectively. FD wafers enable a planar, fully depleted transistor architecture – a breakthrough technology that empowers semiconductor companies to bypass the bulk CMOS roadblock, enabling the efficient design of next-generation, lower power processors for smartphones and mobile computing devices. This architecture is essential in implementing transistor technology that solves – with less process complexity – the scaling, leakage and variability issues that are associated with shrinking CMOS technology starting at 28nm.

About Fully Depleted Value
FD wafers comprise an extremely thin layer of silicon over a buried oxide (BOx) layer. This gives unique properties to the transistors built in this layer. These wafers are ideally suited to mobile and consumer multimedia applications, enabling power savings of up to 40 percent, compared to traditional bulk CMOS, at the same performance level. Similarly, peak performance of processors built on fully depleted wafers can experience up to 60 percent increase, depending on design optimizations. Exceptional performance is maintained at very low power supply (sub-0.7V) so that ultra-low power operation of mobile devices in many use cases can be envisaged. Additionally, fully depleted wafers are processed with standard fab tools sharing many process steps with a conventional, low-power bulk CMOS process. They also save 10 percent of the steps required to fabricate the chips leading to a very competitive cost of finished chip.

About Soitec
Soitec is an international manufacturing company, a world leader in generating and manufacturing revolutionary semiconductor materials at the frontier of the most exciting energy and electronic challenges. Soitec's products include substrates for microelectronics (most notably SOI: Silicon-on-Insulator) and concentrator photovoltaic systems (CPV). The company's core technologies are Smart Cut™, Smart Stacking™ and Concentrix™, as well as expertise in epitaxy. Applications include consumer and mobile electronics, microelectronics-driven IT, telecommunications, automotive electronics, lighting products and large-scale solar power plants. Soitec has manufacturing plants and R&D centers in France, Singapore, Germany, and the United States. For more information, visit: www.soitec.com.

International Media Contact
Camille Darnaud-Dufour
+33 (0)6 79 49 51 43
(any time zone)
camille.darnaud-dufour@soitec.com

Investor Relations
Olivier Brice
+33 (0)4 76 92 93 80
olivier.brice@soitec.com

U.S. Media Contact
Leslie Clavin
Racepoint Group
+1 415 694 6717
lclavin@racepointgroup.com

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